REMARKS

Claims 1-8 still stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Specifically, the Examiner asserts that the present Specification does not sufficiently enable both a "master thread" and a "non-master thread" together in a compiler device having a plurality of threads. Applicants respectfully traverse this rejection because the cited claim features are sufficiently enabled by the Specification.

The Examiner correctly notes that the present Specification describes master and non-master threads on pages 16 and 17. The Examiner is incorrect, however, in his assertion that the Specification "never makes reference to a plurality of threads containing both a master and non-master thread." Furthermore, the implication that the master and non-master threads are *only* described on pages 16-17 is also incorrect. The Specification consistently refers to a plurality of threads, and that one of the plurality is a master thread.

The present Specification first describes, in the "Summary of the Invention" (second to last full paragraph) on page 2, that the compiler device has a plurality of threads, and that this plurality is processed in parallel. The master and non-master threads are then described on page 14, in reference to steps 35-37. Step 35 describes the judgment of whether an active thread of the plurality is the master thread, and steps 36-37 address the case for non-master threads ("a parallelized thread other than the master thread"). Accordingly, the

claim terms cited by the Examiner are sufficiently enabled at least by page 14 of the present Specification and accompanying Fig. 5.

Moreover, these same claim features are also sufficiently enabled by pages 16-17 of the present Specification, contrary to the Examiner's assertion. Examples (1) and (2) address the case where an active thread of the plurality is the master thread, and example (3) describes the case where the active thread is a non-master thread ("not a master thread"). Therefore, the Examiner's assertion that the Specification "never makes reference to a plurality of threads containing both a master and non-master thread" is simply incorrect. Although the specific word "non-master" does not appear in the Specification, the "non-master thread" is clearly described to in the present Specifications as both a thread "other than the master thread" and as a thread "not a master thread." Accordingly, the outstanding Section 112 rejection is inappropriate, and should be withdrawn.

Claims 1 and 5 still stand rejected under 35 U.S.C. 103(a) as being unpatentable over Holzle et al. (U.S. 6,209,066). Applicants respectfully traverse this rejection because the cited reference does not disclose or suggest private interface areas that are dynamically allocated for non-master threads, as in claims 1 and 5 of the present invention, as amended.

Holzle describes a shared memory allocation area 302 that is partitioned into blocks 304 (col. 7, lines 32-38), and which are assigned to threads 306 (col. 7, lines 50-53). The threads 306 may be fast allocating or not (col. 7, lines 50-51), and the designated blocks

304 may be large or small, with large blocks being assigned for a thread that has overflowed its block, or for a thread that may be fast allocating. (See col. 17, line 63 to col. 8, line 29). In other words, Holzle designates private blocks only according to whether a thread is fast allocating or slow, or otherwise for all threads in a plurality of threads (which would include a master thread). Holzle neither teaches nor suggests that the blocks are allocated according to whether a thread is a master thread or a non-master thread.

In contrast, claims 1 and 5 of the present invention as amended recite, among other things, that private interface areas, which are different from the common interface area, are dynamically allocated for non-master threads. Holzle neither teaches nor suggests any such features. The Examiner correctly acknowledged, on page 4 of Paper No. 14, that Holzle does not teach a master thread and a non-master thread, nor does Holzle teach that an interface area is dynamically allocated for the non-master threads. And although the Examiner is correct that master and non-master threads are known in the art, and that a processed thread must have a memory area allocated to it, Applicants note that the Examiner has not even asserted that private interface areas are dynamically allocated according to whether the processed thread is a master or non-master thread.

The present invention does not merely claim master and non-master threads, and interface areas allocated to the threads. Instead, the present invention additionally features that private interface areas, which are different from the common interface area, are dynamically allocated for the non-master threads. Holzle could not teach or suggest that

private interface areas are allocated according to whether a thread, is a master or non-master thread when Holzle fails to even teach master and non-master threads. As discussed above, Holzle teaches the allocation of memory blocks only according to whether or not the thread is fast allocating, or whether it has overflowed its block. Claims 1 and 5 are thus different from Holzle, and the outstanding rejection of these claims based on Holzle should be therefore withdrawn.

Claims 2-4 and 6-8 still stand rejected under 35 U.S.C. 103(a) as being unpatentable over the Schildt reference in view of Holzle. Applicants respectfully traverse this rejection because neither of the recited references, whether taken alone or in combination, discloses or suggests the dynamic allocation of private interface areas according to whether an active thread is a master or non-master thread.

As discussed above, Holzle fails to teach or suggest any dynamic allocation of memory according to whether a thread is the master thread or not. Again, the Examiner expressly acknowledged that Holzle fails to teach master and non-master threads, or an interface area that is dynamically allocated for a non-master thread. Again, the present invention specifically features that the interface area allocated to the non-master thread is a private interface area. Because Holzle fails to teach master and non-master threads or interface areas dynamically allocated for non-master threads, Holzle could not teach or suggest a private interface area allocated to the non-master threads instead of the common interface area, as in independent claims 2 and 6 of the present invention.

Furthermore, the Examiner does not cite Schildt for teaching these features of the present invention. The Examiner relies upon Schildt only for its teachings relating to a compiler converting a source code reference into a dynamically allocated address. Even if the Examiner's reliance upon Schildt in this regard was appropriate (which Applicants do not concede), Schildt still fails to teach or suggest dynamically allocated private interface areas for the non-master threads of a multi-threaded system. The Examiner has acknowledged that Schildt fails to even teach a plurality of threads that use an interface area. Accordingly, because neither of the two cited references teach or suggest all of the features of the present invention, the outstanding rejection of claims 2 (and its dependent claims 3-4) and 6 (and its dependent claims 7-8) is respectfully traversed, and should also be withdrawn.

New claim 9 has been added to recite another combination of features of the present invention. Specifically, independent claim 9 features that the object code of the present invention dynamically allows access to the common interface area according to whether an active thread is the master thread, and accordingly to whether common block information for the interface area is new. Support for these features can be found in the present Specification in the fourth full paragraph of page 14, and the examples described on pages 16-17. Entry, consideration on the merits, and allowance of new claim 9 is respectfully requested.

For all of the foregoing reasons, Applicants submit that this Application, including claims 1-9, is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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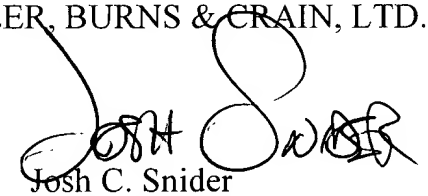
By 

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